

**What Is Claimed Is:**

1           1.    A method for CPU power management and bus optimization  
2    for a system comprising a Northbridge, a bus coupled between the  
3    CPU and the Northbridge, and a Southbridge, the method  
4    comprising the following steps:  
5            setting an initial bus bandwidth, an initial bus frequency,  
6            a bus operating bandwidth and a bus operating  
7            frequency of the bus coupled between the CPU and the  
8            Northbridge, wherein the bus operates at the initial  
9            bus bandwidth and the initial bus frequency;  
10          initializing power management settings of the CPU, the  
11          Northbridge and the Southbridge, wherein the CPU  
12          operates at a CPU operating frequency with a CPU  
13          operating voltage;  
14          obtaining a maximum operating frequency and a maximum  
15          operating voltage for the CPU;  
16          outputting a CPU operating frequency and voltage  
17          adjustment to the Southbridge according to the  
18          maximum operating frequency and the maximum  
19          operating voltage;  
20          output of a bus disconnection signal by the Southbridge to  
21          disconnect the CPU and the Northbridge, initializing  
22          a timer for calculating an elapsed time value;  
23          adjusting the CPU operating frequency and the CPU operating  
24          voltage according to CPU operating frequency and  
25          voltage adjustment;  
26          output of a bus connection signal by the Southbridge when  
27          the elapsed time value reaches a predetermined value;  
28          and

29           reconnection of the CPU and the Northbridge by the bus  
30           according to the bus connection signal, wherein the  
31           bus operates at the bus operating bandwidth and the  
32           bus operating frequency, the CPU operating at the  
33           adjusted CPU operating frequency with the adjusted  
34           CPU operating voltage according to the CPU operating  
35           frequency and voltage adjustment.

1           2.     The method as claimed in claim 1, wherein the bus is  
2           a lightning data transport bus.

1           3.     The method as claimed in claim 1, wherein the bus is  
2           a hyper-transport bus.

1           4.     The method as claimed in claim 1, wherein the bus  
2           disconnection signal and the bus connection signal are output  
3           by a single output terminal.

1           5.     A method for CPU power management and bus optimization  
2           for a system comprising a Northbridge, a bus coupled between the  
3           CPU and the Northbridge, and a Southbridge, the method  
4           comprising the following steps:  
5           setting an initial bus bandwidth, an initial bus frequency,  
6           a bus operating bandwidth and a bus operating  
7           frequency of the bus coupled between the CPU and the  
8           Northbridge, wherein the bus operates at the initial  
9           bus bandwidth and the initial bus frequency;  
10          initializing power management setting of the CPU, the  
11          Northbridge and the Southbridge, wherein the CPU  
12          operates at a first CPU operating frequency with a  
13          first CPU operating voltage;

14 detecting CPU loading and setting a second CPU operating  
15 frequency and a second CPU operating voltage  
16 according to the detection;  
17 outputting a CPU operating frequency and voltage  
18 adjustment to the Southbridge;  
19 output of a bus disconnection signal by the Southbridge to  
20 disconnect the CPU and the Northbridge, initializing  
21 a timer for calculating an elapsed time value;  
22 output of a bus connection signal by the Southbridge when  
23 the elapsed time value reaches a predetermined value;  
24 and  
25 reconnection of the CPU and the Northbridge by the bus  
26 according to the bus connection signal, wherein the  
27 bus operates at the bus operating bandwidth and the  
28 bus operating frequency, and the CPU operates at the  
29 second CPU operating frequency with the second CPU  
30 operating voltage.

1 6. The method as claimed in claim 5, wherein the bus is  
2 a lightning data transport bus.

1 7. The method as claimed in claim 5, wherein the bus is  
2 a hyper-transport bus.

1 8. The method as claimed in claim 5, wherein the bus  
2 disconnection signal and the bus connection signal are output  
3 by a single output terminal.

1 9. The method as claimed in claim 5, further comprising  
2 the following steps:

3 obtaining a maximum operating frequency and a maximum  
4 operating voltage of the CPU; and  
5 setting the second CPU operating frequency and the second  
6 CPU operating voltage according to the maximum  
7 operating frequency and the maximum operating  
8 voltage of the CPU.

1 10. The method as claimed in claim 9, wherein the bus  
2 disconnection signal and the bus connection signal are generated  
3 by asserting and de-asserting a signal output by the  
4 Southbridge.

1 11. A method for CPU power management and bus optimization  
2 for a system comprising a Northbridge, a bus coupled between the  
3 CPU and the Northbridge, and a Southbridge, the method  
4 comprising the following steps:

5 setting an initial bus bandwidth, an initial bus frequency,  
6 a bus operating bandwidth and a bus operating  
7 frequency of the bus coupled between the CPU and the  
8 Northbridge, wherein the bus operates at the initial  
9 bus bandwidth and the initial bus frequency;

10 initializing power management settings of the CPU, the  
11 Northbridge and the Southbridge, wherein the CPU  
12 operates at a first CPU operating frequency with a  
13 first CPU operating voltage;

14 obtaining a maximum operating frequency and a maximum  
15 operating voltage of the CPU;

16 detecting the loading on the CPU and setting a second CPU  
17 operating frequency and a second CPU operating  
18 voltage according to the detection;

19           outputting a CPU operating frequency and voltage  
20           adjustment to the Southbridge according to the  
21           maximum operating frequency and the maximum  
22           operating voltage;  
23           output of a bus disconnection signal by the Southbridge to  
24           disconnect the CPU and the Northbridge, initializing  
25           a timer for calculating an elapsed time value;  
26           output of a bus connection signal by the Southbridge when  
27           the elapsed time value reaches a predetermined value;  
28           and  
29           reconnection of the CPU and the Northbridge by the bus  
30           according to the bus connection signal, wherein the  
31           bus operates at the bus operating bandwidth and the  
32           bus operating frequency, and the CPU operates at the  
33           second CPU operating frequency with the second CPU  
34           operating voltage.

1           12. The method as claimed in claim 11, wherein the bus is  
2           a lightning data transport bus.

1           13. The method as claimed in claim 11, wherein the bus is  
2           a hyper-transport bus.

1           14. The method as claimed in claim 11, wherein the bus  
2           disconnection signal and the bus connection signal are output  
3           by a single output terminal.

1           15. The method as claimed in claim 14, wherein the bus  
2           disconnection signal and the bus connection signal are generated  
3           by asserting and de-asserting a signal output by the  
4           Southbridge.